TR 901008-4

Quarterly Report on

"Development and Testing of Radiation and Electromagnetic Pulse Hardened Silicon Carbide Based Electronics"

Contract Number:
N00014-90-C-0037

For the Period:
June 1, 1990 - August 31, 1990

Submitted to:

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Ref: Contract N00014-90-C-0037

Source of Funding:

OSD/SDIO/IST

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September 19, 1990

I. Summary

There were three primary objectives ~~for this reporting period.~~ The first was the reverse avalanche testing of diodes exhibiting (a) microplasma dominated breakdown, (b) a combination of microplasma and bulk avalanche breakdown and (c) bulk avalanche breakdown only. These glass encapsulated devices were tested at ~1 μs, ~10 μs and 100 μs. pulses. The second objective was to fabricate and characterize Shockley diodes in chip form showing proper breakdown in forward and reverse bias and a forward bias turn-on of ~2.6 V. The third objective was to fabricate and characterize 6H-SiC JFET structures in chip form.

II. Avalanche Energy Testing (AET) of Diodes

To simulate the effects of an electromagnetic pulse (EMP) on a p-n junction device, reverse bias AET was performed. The axial lead diodes employed were glass encapsulated in a DO-204AM, hermetically sealed and voidless package. Diodes showing three types of reverse breakdown characteristics were selected for testing. The devices exhibited (a) microplasma dominated breakdown, (b) a combination of microplasma and bulk avalanche breakdown and (c) bulk avalanche breakdown. The breakdown voltage of the diodes tested ranged from 375-500 V.

Pulse widths were controlled at approximately 3 levels; 1, 10 and 100 μs. The test circuits used to apply the 1 μs pulse and both the 10 and 100 μs pulses are shown schematically in Figs. 1a and 1b, respectively. In test, the diodes exibited a sharp square voltage and current pulse. The voltage was clamped by the diode whereas the current in avalanche was increased to the point where a short circuit developed in the diode. This point was taken as the point of failure for the part. The sample size for each diode type was 4 pieces. The summary of results is given in Table I below

The failure mechanism for these devices has not been determined. After pulsing to the point of failure, the diode still shows rectification characteristics with a large linear leakage current caused by the high power pulse. The breakdown may be due to failure of the SiO_2 passivation layer. This phenomenon is presently being investigated by using three different oxide thicknesses at 400 V and testing low voltage devices (<100 V) where the influence from the oxide is minimized.

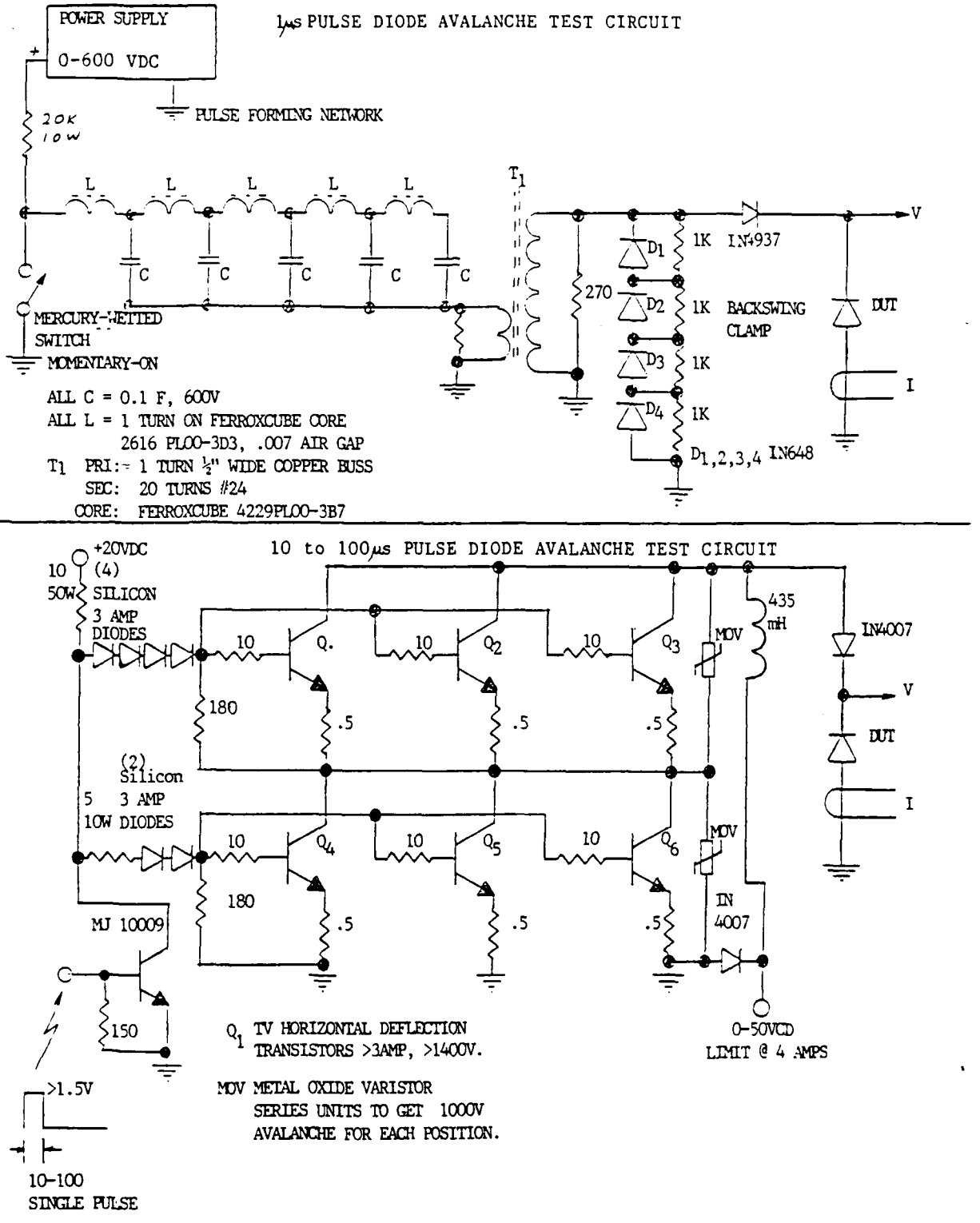

Figure 1. Schematic drawing showing circuits designed for performing the 1μs pulses (top) and 10 to 100 μs pulses (bottom).

Table I. AET Summary of Results For 6H-SiC Diodes

Type(#)	Voltage(V)	Current(A)	Time(μs)	Energy(mJ)	Power Density(kW/cm^2)
A1	500	<0.1	~1	~0	~0
A2	500	<0.1	~1	~0	~0
A3	416	2.8	2.0	2.3	224
A4	410	<0.1	~1	~0	~0
A5-A12	375-500	~0	10,100	~0	~0
B1	448	1.44	1	0.6	124
B2	416	16.4	1.5	10.2	1315
B3	472	6.9	1.9	6.2	628
B4	440	15.6	1.5	10.3	1325
B5	384	0.92	10	3.5	68.1
B6	424	2.10	10	8.9	171.6
B7	480	0.80	10	3.8	74.0
B8	440	2.76	14	17.0	234.0
B9	408	0.22	90	8.2	17.3
B10	392	0.20	100	7.8	15.1
B11, B12	375-500	~0	100	~0	~0
C1	420	13.0	1.6	8.7	1052
C2	408	23.0	1.4	13.1	1808
C3	376	17.6	1.5	9.9	1275
C4	480	18.8	1.5	13.5	1739
C5	440	0.8	13.5	4.7	67.8
C6	400	2.56	10	10.2	197.3
C7	385	3.50	22.5	30.3	260.0
C8	408	3.70	14	21.1	291.0
C9	432	1.35	100	58.3	112.4
C10	384	1.20	100	46.1	88.8
C11	488	1.30	100	63.4	122.2
C12	456(soft)	0.80	100	36.5	70.3

It is clear from the results in Table I, that the devices exhibiting bulk avalanche are generally more durable and predictable when subjected to AET. The type A devices, which breakdown via microplasmas, are very unstable and poor in avalanche. The type B devices showed a range from very good to very poor characteristics in AET at the 1 and 10 μs pulses. At 100 μs pulses, their tolerance to AET was quite poor.

Figure 2 shows a plot of power per unit area (P/A) in kW/cm^2 versus pulse time (t) in μs for typical silicon diodes, the theoretical limit for SiC diodes and the experimental results of the top devices in this study. In the Dec. 7, 1989-Feb. 28, 1990 report, the theoretical limit for P/A in SiC diodes was given as:

$$P/A_{max} \sim 9810\ t^{-1/2} \qquad \text{Eqn. 1}$$

The experimental results of this research show the relationship:

$$P/A_{exp} \sim 1805\ t^{-0.63} \qquad \text{Eqn. 2}$$

This is an improvement over silicon devices by a factor of 1.8-3.2 in the pulse times tested (1-100 μs). However, it is still a factor of 5.4-9.9 below the theoretical limit (in the same pulse time range) for SiC. For this reason, it is postulated that the principle mechanism of failure for the present devices is not localllized melting of SiC at the junction, but rather breakdown of the junction passivation layer.

III. Shockley Diode Characterization

In this reporting period, a number of Shockley diodes were fabricated and characterized. The basic device was constructed using a n-type 6H-SiC substrate with four epitaxial layers (1) $n_1 \sim 3x10^{18}$ cm^{-3}, thickness (t)=0.2 μm, (2) $p_1=1\text{-}4x10^{16}$ cm^{-3}, t=3.3 μm, (3) $n_2 \sim 1x10^{18}$ cm^{-3}, t=1 μm and (4) $p_2=4\text{-}10x10^{18}$ cm^{-3}, t=0.8 μm. The carrier concentration of each epitaxial layer was measured using a mercury probe in conjunction with a capacitance-voltage (C-V) system. The device configuration is summarized in Fig. 2.

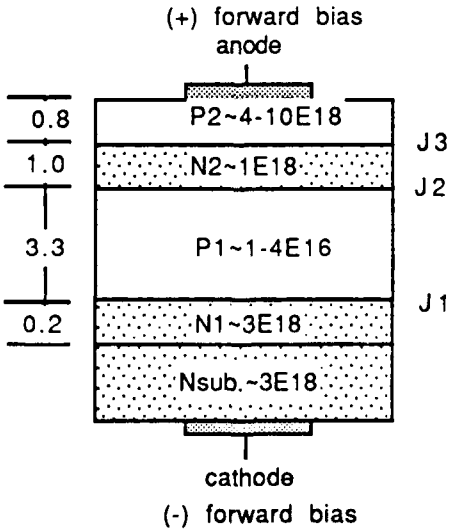

Figure 2. Schematic diagram of Shockley diode structure built during this reporting period.

Figure 3 shows a resulting current-voltage (I-V) plot of a device with a P_1 level of $1.3x10^{16}$ cm^{-3} (determined by C-V measurement of device). In the reverse biased mode, junctions J_1 and J_3 are reverse biased and J_2 is forward biased. In this configuration (see Fig. 2), most of the voltage is dropped across J_1 and depletion predominantly occurs in layer P_1, the layer with the lesser carrier concentration.

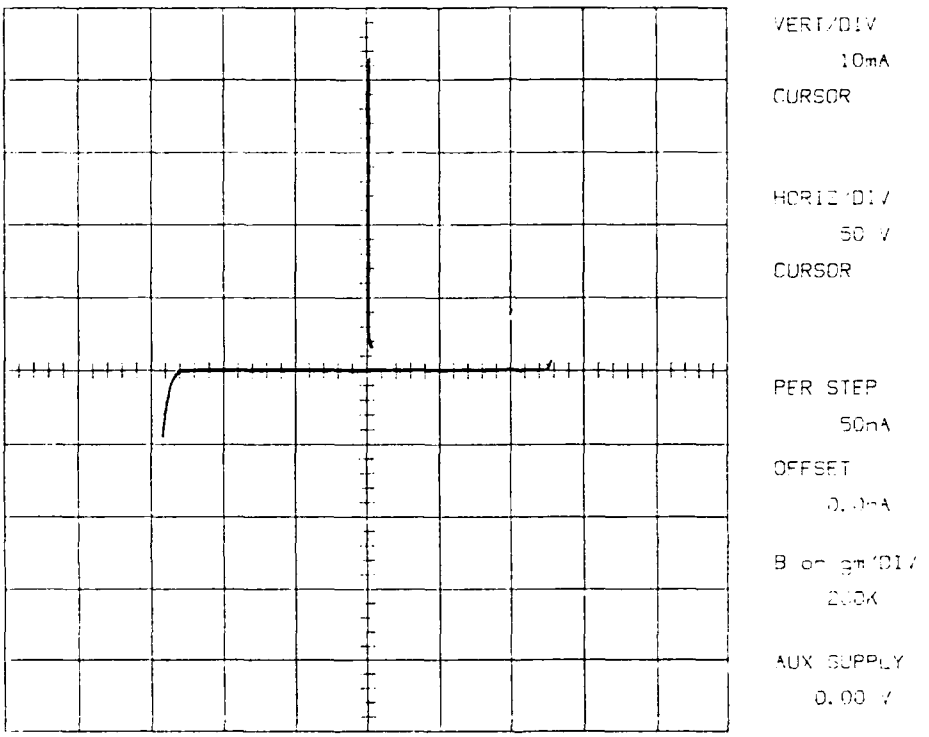

Figure 3. The forward and reverse bias I-V characterisics of a 6H-SiC Shockley diode with a device configuration as shown in Fig. 2. The carrier concentration in P_1 is $1.3x10^{16}cm^{-3}$ and the epitaxial layer thickness is 3.3 μm. Breakdown occurs via punch-through.

The breakdown characteristics are controlled by this junction and breakdown voltage (V_{br}) by the carrier density in P_1 whereby avalanche multiplication breakdown mechanism will occur or the epitaxial layer thickness whereby a punch-through breakdown can occur. Since the epitaxy layer (P_1) thickness is insufficient

for the given carrier concentration to achieve avalanche, punch-through is observed. The punch-through voltage (V_{PT}) can be calculated for a one-sided abrupt junction as:

$$V_{PT}=V_{bi}-qP_1(x_p)^2/2\varepsilon_o k \qquad \text{Eqn. 3}$$

where V_{bi} is the built-in potential of the junction (~2.6 V), q is the electron charge (1.6×10^{-19} C), x_p is the depletion depth at punch-through (thickness of P_1), ε_o is the permittivity of free space (8.85×10^{-14} F/cm) and k is the dielectric constant of the material (10 for SiC). Using the values of of P_1 and x_p above, V_{PT} is given as:

$$V_{PT}=2.6V-[(1.6\times10^{-19}C)(1.3\times10^{16}cm^{-3})(3.3\times10^{-4}cm)^2/2(8.85\times10^{-14}F/cm)(10)]$$

$$\therefore \quad V_{PT}\sim-125\ V$$

This calculated value of V_{PT} closely matched the measured reverse bias breakdown voltage value for the Shockley diode above.

In forward bias (P_2 is positively biased and N_{sub} negatively biased), only J_2 is reverse biased. Most of the voltage is dropped across this junction and the forward breakover voltage, V_{bf}, is again controlled by the carrier density and thickness of P_1. Hence, the value of V_{bf} should be equal to V_{PT}, assuming uniform doping across the epitaxial layer. As shown in Fig. 3, the two voltage values are very similar. Once this voltage is reached, there are three forward biased junctions and the device conducts. The total forward voltage drop is approximately equal to the sum of the voltage drops in J_1, J_2 and J_3. Since the potential at J_2 (V_2) is opposite in polarity to both J_1 and J_2, the net forward voltage drop is approximately equal to the voltage drop across a single junction. As with a SiC single junction diode, this voltage should be approximately 2.6 V. Upon turn-on, the current should increase linearly with voltage.

The forward bias I-V characteristics upon turn-on for the above Shockley diode are shown in Fig. 4. The turn-on voltage shown is ~2.6 V and the on resistance is 5 Ω. From this data it is apparent that the junction potentials were additive, two positive (5.2 V) and one negative (2.6 V) yielding a net 2.6 V. Since the Shockley diode operated as modelled, a SiC thyrister can now be fabricated.

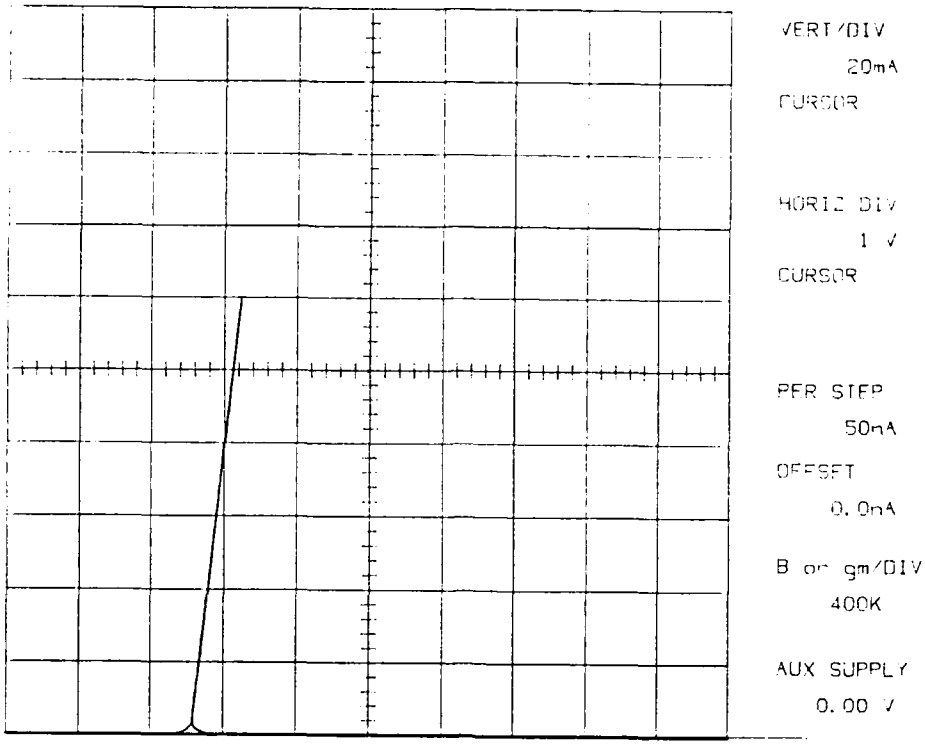

Figure 4. Forward bias I-V characteristics of the 6H-SiC Shockley diode shown in Fig. 3 showing a turn-on voltage of 2.6 V.

IV. Junction Field-Effect Transistors

The fabrication of the first set of 6H-SiC JFETs was completed during this reporting period and their I-V characteristics were measured. The cross-sectional design used for these devices is shown in Fig. 5. The source and drain contacts of the buried gate JFETs are on top of the wafer and the gate, defined by the fine line trench between the source and drain, is controlled through the p-type substrate. Four different gate lengths were fabricated. All of these had a source contact - drain contact distance of 8 μm.

The epilayers for these devices were grown in three different steps, with the carrier concentration being measured by C-V after every growth. The first layer, or gate layer, was 3 μm thick and was heavily doped to $p = 2\text{-}4 \times 10^{18}$ cm^{-3}. The n-type conducting channel was 0.4 μm thick and was doped in the range of

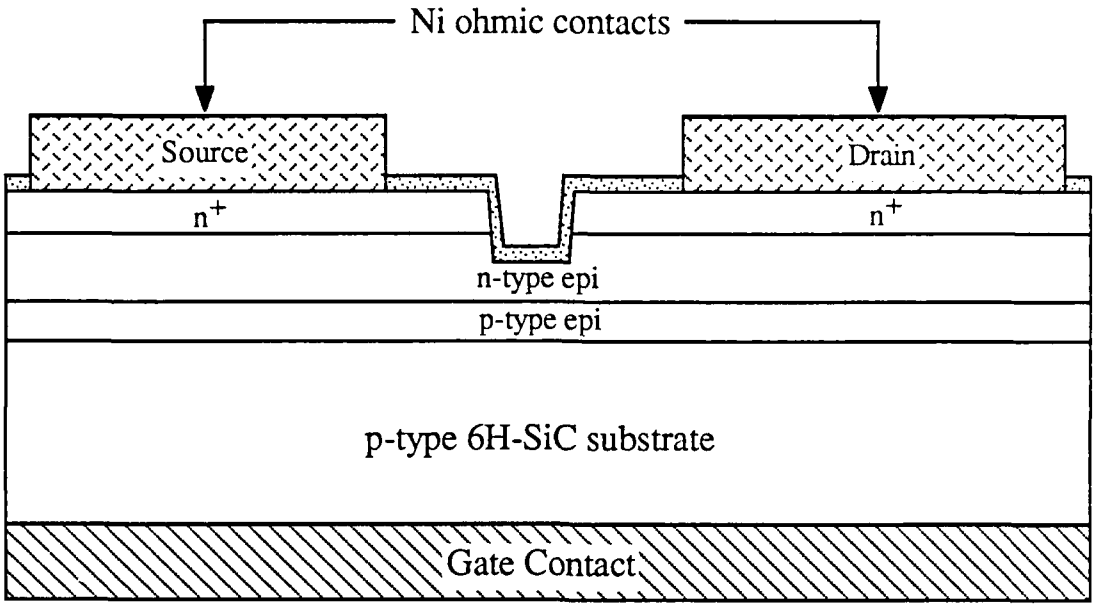

Figure 5. Cross-sectional view of the present design for a buried-gate 6H-SiC JFET.

1.4-1.7x10^{17} cm^{-3}. The top n^+ layer was 0.3 μm thick and doped to n = 1-2x10^{19} cm^{-3}. Device processing involved the following steps. Using reactive ion etching (RIE), a mesa was etched down to the buried p-type layer to confine the current. Then the fine line trench was etched across the mesa that cuts through the top n^+ layer and down to the desired depth in the n-type conducting channel, thus defining the actual gate length. This gate level photolithography step presented some problems because of difficulties in obtaining fine line widths, but gate lengths in the range of 1.5 to 2.5 μm were achieved. The samples were then oxidized to passivate the surfaces, and the source and drain contacts were subsequently deposited and patterned. Finally, the p-type ohmic contact metal was deposited on the backside of the wafer, and the contacts were annealed.

The I-V characteristics of a 6H-SiC buried gate JFET are shown in Fig. 6. This device had a gate length of 2 μm and a gate width of 1 mm. Source-drain voltages of 40 V were achieved. The maximum transconductance of this device was 15 mS/mm at V_G = +2 V and V_{DS} = 40 V. The maximum gate leakage current with V_G = +2 V was 2 mA, due to the fact that the gate diode is within 0.5 V of overcoming its built-in potential. The gate leakage at the other gate values was in the range of 100 μA at V_{DS} = 40 V. The subthreshold leakage current at V_{DS} = 40 V and V_G = -2 V was 200 μA. Although the

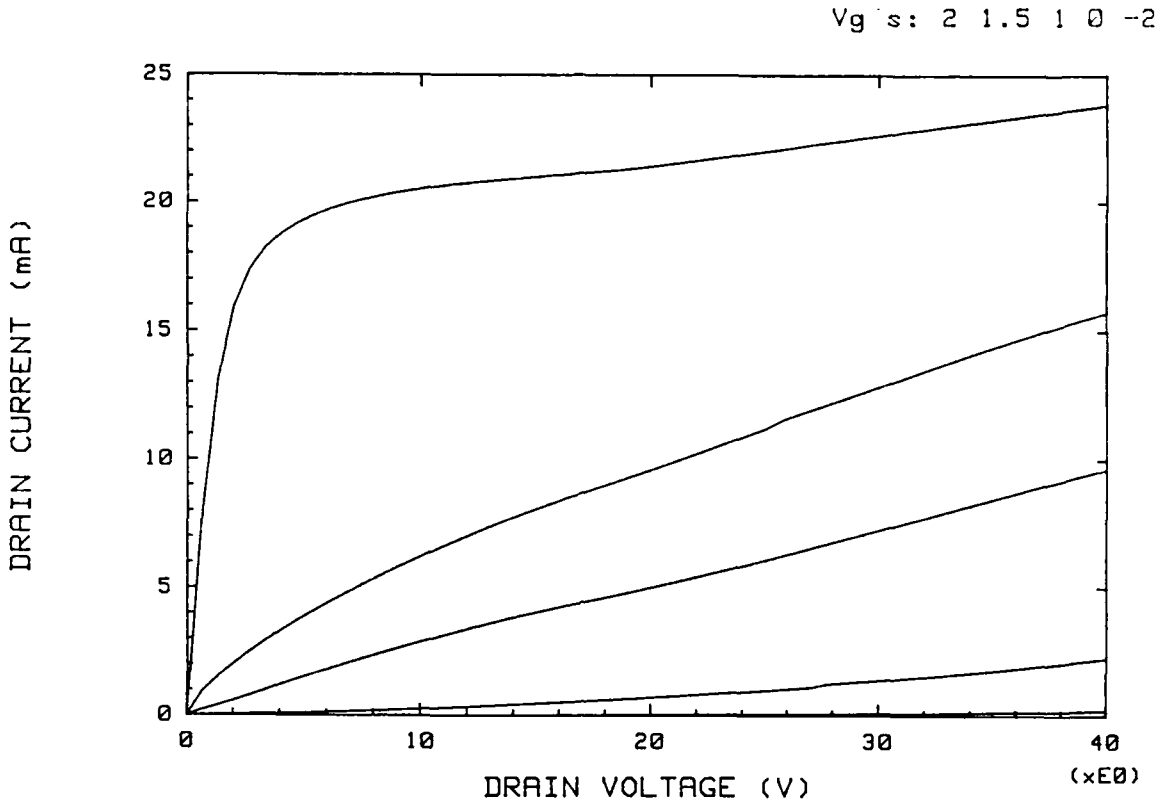

Figure 6. Current-voltage characteristics for a 6H-SiC JFET at room temperature. The gate length and width were 2 μm and 1 mm, respectively.

doping and thickness of these samples should have resulted in pinch-off voltages in the range of V_p = -10 V, these devices displayed much smaller values of V_p. The device in Fig. 6 actually works as an enhancement mode device with a V_p = -0.9 V. In fact, some of the channels were fully depleted by the 2.5 V built-in potential of the buried p^+-n junction and showed no transistor action.

It is obvious from the I-V results that the "effective" thickness of the conducting channel was much thinner than expected. Since the thickness of the n-type layer is known from the growth time and the carrier concentration at the top of the conducting channel was measured by Hg probe, it is apparent that the "effective" thickness was greatly decreased because a large amount of Al diffused from the p^+ layer into the n-type channel. This diffusion probably did not shift the position of

the pn junction very far, but did heavily compensate part of the adjoining n-type layer. Because this compensation would decrease the n-type carrier concentration near the junction, the depletion region from the pn junction would extend much further into the channel, resulting in pinch-off voltages nearer to 0 V. This effect has not been observed in other depletion-mode devices fabricated at Cree, such as MESFETs, because the buried p-type layer is very lightly doped, acting only as an insulating layer and not as a gate.

V. Future Plans

The next step being taken to verify the EMP hardness of SiC junctions is to (a) produce and test low breakdown voltage parts (<100 V) and (b) fabricate ~400 V avalanche parts with various passivation types and thicknesses. In the former case the influence of the passivation layer is minimized and in the latter more dominant. The types of passivation layers tested will be wet and dry SiO_2 with various thicknesses.

With the successful fabrication of the Shockley diode, a gated device, or thyrister will now be designed. This will likely utilize an interdigitated geometry.

Further JFET devices will be grown and fabricated. The n-type channel thicknesses will be increased to offset the effect of Al diffusion from the p^+ gate layer. Also, the n-type carrier concentrations will be increased to decrease the effect of Al compensation. Given the high transconductances measured for the devices in discussed in this report, future devices should show very promising high power characteristics.